

PATENT 8040-1022

## IN THE U.S. PATENT AND TRADEMARK OFFICE

In re application of

Hirotaka NAKANO et al.

Conf. 9420

Application No. 09/855,723

Group 2825

Filed May 16, 2001

Examiner Magid Y. Dimyan

SYSTEM OF MANUFACTURING SEMICONDUCTOR INTEGRATED CIRCUIT BY HAVING A CLIENT CONNECTED TO A MANUFACTURER VIA TWO-WAY COMMUNICATION

## INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

In compliance with Rules 1.97 and 1.98, and in ful-fillment of the duty of disclosure under Rule 1.56, the accompanying documents, copies of which are attached to this statement, are made of record on the enclosed Form PTO-1449.

A concise explanation of the relevance of these items is that these references were cited by the Japanese Patent Office in the corresponding Japanese Application Serial No. 2000-142918, filed May 16, 2000. A copy of the Japanese Official Action in which they were cited is attached hereto, with what is believed to be the pertinent portion enclosed in a wavy line. An English translation of the enclosed portion is also attached hereto.

Under the provisions of 37 CFR 1.97(e), the undersigned hereby certifies that each item of information con-

Docket No. 8040-1022 Appln. No. 09/855,723

tained in this Information Disclosure Statement was first cited in any communication from a foreign Patent Office in a counterpart foreign application not more than three months prior to the filing of this Statement.

Please charge the fee of \$180 required by 37 C.F.R. §1.17(p) to Deposit Account No. 25-0120.

Respectfully submitted,

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January 3, 2005

INFORMATION DISCLOSURE CITATION			Attorney Docket No.: 8040-1022		Application No.: 09/855,723			
	IN AN APPLICATI		Applicant: Hirotaka NAKANO et al.					
Use several sheets if necessary)			Filing Date: May 16, 2001		Group Art Unit: 2825			
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	JP 2000-76320	03/14/2000	Japan Japan					
	JP 11-15520	01/22/1999						
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<sup>\*</sup> Abstract provided for the Examiner's convenience